CLAIMS:

What is claimed is:

1. A method in a data processing system for processing instructions, the method comprising:

responsive to receiving an instruction at a processor in the data processing system, determining whether an indicator is associated with the instruction;

enabling counting, by the processor, of each first event associated with a primary metric of the execution of the instruction if the indicator is associated with the instruction, wherein the processor autonomically increments the count of the first events associated with the primary metric of the execution of the instruction in a first hardware counter;

determining if the count of the first events associated with the primary metric of the execution of the instruction stored in the first hardware counter satisfies a predetermined relationship with a threshold value; and

enabling counting, by the processor, of each second event associated with a secondary metric of the execution of a portion of code associated with the instruction, wherein the processor autonomically increments the count of the second events associated with the secondary metric of the execution of a portion of code associated with the instruction in a second hardware counter.

2. The method of claim 1, wherein the instruction is received in an instruction cache in the processor.

3. The method of claim 1, wherein the indicator is stored in a performance instrumentation shadow cache and wherein the processor checks the performance instrumentation shadow cache to determine whether the indicator is associated with the instructions.

4. The method of claim 1, wherein the instruction is received in a bundle by an instruction cache in the processor and wherein the indicator comprises at least one spare bit in a field in the bundle.

5. The method of claim 1, wherein the indicator is a separate instruction.

6. The method of claim 1, wherein the first events include at least one of an entry into a module, an exit from a module, an entry into a subroutine, an exit from a subroutine, an entry into a function, an exit from a function, a start of input/output, a completion of input/output, and the execution of the instruction.

7. The method of claim 1, wherein determining whether an indicator is associated with the instruction comprises:

determining, by an instruction cache, whether the indicator is present in a field within the instruction.

8. The method of claim 1, wherein the enabling the counting of first events includes sending a first signal to a performance monitor unit, wherein the performance monitor unit counts each first event associated with execution of the instruction using the first hardware counter, and wherein enabling the counting of second events includes sending a second signal to a performance monitor unit, wherein the performance monitor unit counts each second event associated with execution of a portion of code associated with the instruction using the second hardware counter.

9. The method of claim 1, wherein the first hardware counter is a combined counter value hardware counter that stores a combined count from a plurality of other hardware counters.

10. The method of claim 1, wherein enabling counting, by the processor, of each second event associated with a secondary metric of the execution of a portion of code associated with the instruction includes:

generating an interrupt in response to a determination that the count of the first events meets or excess the threshold value; and

sending the interrupt to an interrupt handler of a performance monitoring application, wherein the interrupt handler of the performance monitoring application initiates counting of each second event associated with a secondary metric of the execution of a portion of code associated with the instruction.

11. The method of claim 10, wherein the interrupt handler instruments other instructions in the portion of code associated with the instruction to include the indicator.

12. The method of claim 10, wherein the interrupt handler initiates the second hardware counter and associates the second hardware counter with the portion of code.

13. The method of claim 1, wherein the portion of code associated with the instruction includes at least one of instructions of a same class of instructions as the instruction and instructions within a same method or routine as the instruction.

14. The method of claim 1, wherein the first metric is different from the second metric.

15. A computer program product in a computer readable medium for processing instructions comprising:

first instructions for responsive to receiving an instruction at a processor in the data processing system, determining whether an indicator is associated with the instruction;

second instructions for enabling counting, by the processor, of each first event associated with a primary metric of the execution of the instruction if the indicator is associated with the instruction, wherein the

processor autonomically increments the count of the first events associated with the primary metric of the execution of the instruction in a first hardware counter;

third instructions for determining if the count of the first events associated with the primary metric of the execution of the instruction stored in the first hardware counter satisfies a predetermined relationship with a threshold value; and

fourth instructions for enabling counting, by the processor, of each second event associated with a secondary metric of the execution of a portion of code associated with the instruction, wherein the processor autonomically increments the count of the second events associated with the secondary metric of the execution of a portion of code associated with the instruction in a second hardware counter.

16. The computer program product of claim 15, wherein the instruction is received in an instruction cache in the processor.

17. The computer program product of claim 15, wherein the indicator is stored in a performance instrumentation shadow cache and wherein the processor checks the performance instrumentation shadow cache to determine whether the indicator is associated with the instructions.

18. The computer program product of claim 15, wherein the instruction is received in a bundle by an instruction

cache in the processor and wherein the indicator comprises at least one spare bit in a field in the bundle.

19. The computer program product of claim 15, wherein the indicator is a separate instruction.

20. The computer program product of claim 15, wherein the first events include at least one of an entry into a module, an exit from a module, an entry into a subroutine, an exit from a subroutine, an entry into a function, an exit from a function, a start of input/output, a completion of input/output, and the execution of the instruction.

21. The computer program product of claim 15, wherein the first instructions include:

instructions for determining, by an instruction cache, whether the indicator is present in a field within the instruction.

22. The computer program product of claim 15, wherein the second instructions for enabling the counting of first events include instructions for sending a first signal to a performance monitor unit, wherein the performance monitor unit counts each first event associated with execution of the instruction using the first hardware counter, and wherein enabling the counting of second events includes sending a second signal to a performance monitor unit, wherein the performance monitor

unit counts each second event associated with execution of a portion of code associated with the instruction using the second hardware counter.

23. The computer program product of claim 15, wherein the first hardware counter is a combined counter value hardware counter that stores a combined count from a plurality of other hardware counters.

24. The computer program product of claim 15, wherein the fourth instructions for enabling counting, by the processor, of each second event associated with a secondary metric of the execution of a portion of code associated with the instruction include:

instructions for generating an interrupt in response to a determination that the count of the first events meets or excess the threshold value; and

instructions for sending the interrupt to an interrupt handler of a performance monitoring application, wherein the interrupt handler of the performance monitoring application initiates counting of each second event associated with a secondary metric of the execution of a portion of code associated with the instruction.

25. The computer program product of claim 24, wherein the interrupt handler instruments other instructions in the portion of code associated with the instruction to include the indicator.

26. The computer program product of claim 24, wherein the interrupt handler initiates the second hardware counter and associates the second hardware counter with the portion of code.

27. The computer program product of claim 15, wherein the portion of code associated with the instruction includes at least one of instructions of a same class of instructions as the instruction and instructions within a same method or routine as the instruction.

28. The computer program product of claim 15, wherein the first metric is different from the second metric.

29. An apparatus for processing instructions, the method comprising:

means for determining whether an indicator is associated with the instruction in response to receiving an instruction at a processor in the data processing system,;

means for enabling counting, by the processor, of each first event associated with a primary metric of the execution of the instruction if the indicator is associated with the instruction, wherein the processor autonomically increments the count of the first events associated with the primary metric of the execution of the instruction in a first hardware counter;

means for determining if the count of the first events associated with the primary metric of the execution of the instruction stored in the first hardware

counter satisfies a predetermined relationship with a threshold value; and

means for enabling counting, by the processor, of each second event associated with a secondary metric of the execution of a portion of code associated with the instruction, wherein the processor autonomically increments the count of the second events associated with the secondary metric of the execution of a portion of code associated with the instruction in a second hardware counter.